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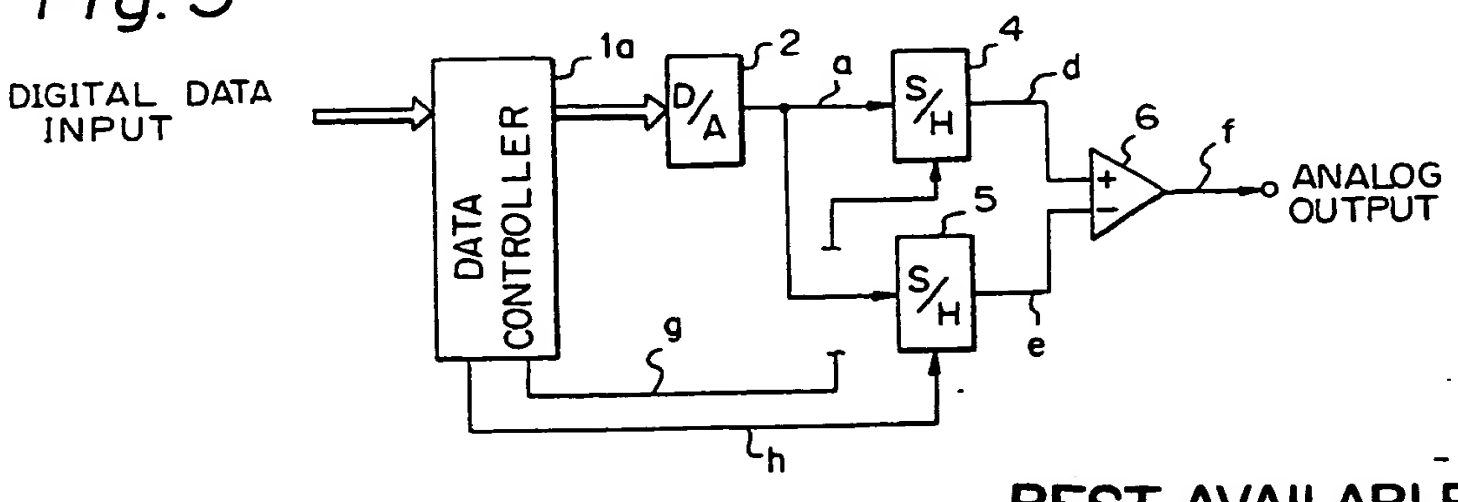
(54) D/A conversion circuit.

(57) The invention provides a D/A conversion circuit in which the polarities of a series of input digital data are reversed (1a) with every other data block, and the original digital data and the reversed digital data are alternately D/A converted (2). An output analog signal (f) is obtained by subtraction (6) between the two D/A converted analog signals (d, e).

With the above-mentioned arrangement, the D/A conversion circuit has a dynamic range equivalent to that using two D/A converters even with a single D/A converter.

Fig. 3



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D/A CONVERSION CIRCUIT

The present invention relates to the improvement of a D/A conversion circuit.

An example of a conventional D/A conversion circuit is explained in the following, while referring to Fig. 1.

Referring now to Fig. 1, a series of digital data group which bear level signal information such as audio signal data of a 16 bit L or R channel decoded at an audio signal processor of a CD player etc. are supplied to a data controller 1.

The data controller 1 supplies the supplied digital data to a D/A converter 2 as non-reversed data and also it obtains reversed data which are obtained by reversing only the polarity of each block of supplied digital data and supplies the reversed data to a D/A converter 3 in synchronization with the supply of corresponding non-reversed data to the D/A converter 2.

The D/A converter 2 generates an output voltage "a" with a level corresponding to the polarity and the value of the non-reversed data, and supplies it to a sample-hold circuit 4. The D/A converter 3 generates an output voltage "b" with a level corresponding to the polarity and the value of the reversed data, and supplies it to a sample-hold circuit 5.

The sample-hold circuits 4 and 5 receive and hold the output voltages of the D/A converters corresponding to the timing clock pulses "C" corresponding to the data supplied from the data controller 1. The holding output "d" of the sample-hold circuit 4 is supplied to the positive-phase input terminal of a differential amplifier 6, and the holding output "e" of the sample-hold circuit 5 is supplied to the negative phase input terminal of the differential amplifier 6.

The differential amplifier 6 generates a voltage "f" corresponding to the level difference between the two voltages held by the sample-hold circuits 4 and 5.

Next, the operation of a device is described referring to Fig. 2 in the following.

When a series of digital data group are supplied to the data controller 1, the data controller 1 obtains two kinds of data having the same absolute values and opposite polarities concerning the digital data and supplies them to D/A converters 2 and 3. Therefore, the outputs "a" and "b" of the D/A converters 2 and 3 vary complementarily as shown in Fig. 2A and Fig. 2B.

Two outputs "a" and "b" of these D/A converters are held as shown in Fig. 2D and Fig. 2E by sample-hold circuits 4 and 5 which remove glitch noise operating in synchronization with the timing clock pulses "c". The differential amplifier 6 generates an output "f" which is proportional to the level difference between the holding outputs "d" and "e" of sample-hold circuits 4 and 5.

In the arrangement as mentioned in the above, there is a merit that the D/A conversion output "f" has a double dynamic range as shown in Fig. 2F in comparison with the D/A conversion output characteristics when a single D/A converter is used as shown in Fig. 2A.

Two units of expensive D/A converters are used in the above constitution. Four units of D/A converters are needed in total in the case a digital audio device which generally have 2-channel signal processors, which cannot be neglected from the point of view of manufacturing cost. It is also a demerit that when the characteristics of these two D/A converters to be used in a pair are not identical, distortion occurs in the conversion output.

An object of the present invention is to provide a D/A conversion circuit in which a double dynamic range can be obtained even with a single D/A converter.

To achieve the above-mentioned object, a D/A conversion circuit in a first embodiment of the invention comprises a reversal means for reversing the polarities of every other data block in a series of input digital data group and for supplying them to a D/A converter, sample-hold means for holding two conversion output levels corresponding to input digital data blocks adjacent to each other of the above-mentioned D/A converter, and a subtraction means for obtaining a level difference between the two conversion output levels.

A D/A conversion circuit in a second embodiment of the invention comprises a positive and negativ data creation means for alternately supplying reversed data obtained by reversing the polarities of a series of input digital data group and non-reversed data in the input digital data group with every other data block, an sample-hold means for holding two conversion output levels corresponding to the input digital data blocks adjacent to each other of the D/A converter, and a subtraction means for obtaining the level difference between the two conversion output levels.

Embodiments of the invention will now be described in more detail, by way of example only and with reference to the accompanying drawings, in which :-

Fig. 1 is a block diagram showing an example of a conventional type device. Fig. 2 is an explanatory diagram of the operation of a conventional type device. Fig. 3 is a block diagram showing an embodiment of the pr sent invention. Fig. 4 is an explanatory diagram of the operation of the em-

bodiment. Fig. 5 is a block diagram showing another embodiment. Fig. 6 is an explanatory diagram of another embodiment.

An embodiment according to the present invention will be explained referring to Fig. 3 in the following. Similar symbols are given to the parts of a device shown in Fig. 3 which correspond to those of the device shown in Fig. 1.

In Fig. 3, a data controller 1a converts the polarities of data blocks with every other block of data in the supplied series of digital data group and supplies them to a D/A converter 2. The D/A converter 2 alternately converts non-reversed data whose polarities are not reversed and reversed data whose polarities are reversed into voltage values, and generates output voltage "a" as shown in Fig. 4A and supply it to sample-hold circuits 4 and 5.

The sample-hold circuit 4 receives and holds the output of the D/A converter 2 corresponding to the supplying condition of non-reversed data to the D/A converter 2 in synchronization with timing clock pulses "g" as shown in Fig. 4B supplied from the data controller 1a. The sample-hold circuit 5 receives and holds the output of the D/A converter 2 corresponding to the supplying condition of reversed data to the D/A converter 2 in synchronization with timing clock pulses "h" as shown in Fig. 4C supplied from the data controller 1a. Therefore the holding outputs "d" and "e" of the sample-hold circuits 4 and 5 corresponding to the output of the D/A converter 2 shown in Fig. 4A are respectively as shown in Fig. 4D and Fig. 4E.

The output "f" of a differential amplifier 6 based on the outputs "d" and "e" of the sample-hold circuits has, as shown in Fig. 4F, a dynamic range in the output level which is double a single D/A converter shown in Fig. 2A.

Another embodiment will be explained while referring to Fig. 5 in the following. Similar symbols are given to the parts of a device shown in Fig. 5 which correspond to those of the device shown in Fig. 3.

In Fig. 5, a data controller 1b supplies the supplied digital data to one input terminal of a multiplexer 10 as non-reversed data, and also the data controller 1b obtains the reversed data by reversing only the polarities of the supplied digital data and supplies them to the other terminal of the multiplexer 10 in synchronization with the supply of corresponding non- reversed data to the multiplexer 10.

The multiplexer 10 relays non-reversed data and reversed data alternately to the D/A converter 2 in synchronization with the supply period of input digital data supplied from the data controller 1b and in response to a switching signal having the half period of the supply period. In this way, the digital data quantity supplied to the D/A converter 2 is doubled.

The D/A converter 2 converts the digital data whose polarities are alternately reversed into a voltage "a" as shown in Fig. 6A and supplies it to the sample-hold circuits 4 and 5.

The sample-hold circuit 4 receives and holds the output of the D/A converter 2 in synchronization with timing-clock pulses "i" as shown in Fig. 6B which are generated corresponding to the supplying condition of non-reversed data from the data controller 1b to the multiplexer 10. The sample-hold circuit 5 receives and holds the output of the D/A converter 2 in synchronization with timing-clock pulses "j" as shown in Fig. 6C which are generated corresponding to the supplying condition of reversed data from the data controller 1b to the multiplexer 10. Therefore the holding outputs D and E of sample-hold circuits 4 and 5 corresponding to the output "a" of the D/A converter 2 as shown in Fig. 6A are respectively as shown in Fig. 6D and Fig. 6E.

The output "f" of the differential amplifier 6 based on the outputs "d" and "e" of these sample-hold circuits has a double dynamic range as shown in Fig. 6F and moreover it shows twice oversampled characteristics in comparison with the output of a single D/A converter as shown in Fig. 2A.

With the above-mentioned arrangement according to the present invention using a single D/A converter, the similar or better D/A conversion characteristics can be obtained in comparison with the case where two D/A converters are used as in the case of a conventional device.

It is also possible to make the data controller 1b shown in Fig. 5 have the function of the multiplexer 10 shown in the same drawing.

As described in the above, in a D/A conversion circuit according to the present invention, the polarities of input digital data blocks are alternately reversed and the data are supplied to a single D/A converter to obtain two D/A conversion outputs corresponding to adjacent conversion input data blocks, and the difference between these two conversion outputs is made to be the output of the D/A converter. It is therefore made possible to obtain a double dynamic range of the original dynamic range of a D/A converter by using a single D/A converter and also to provide an economical D/A converter by reason that there is no need to obtain D/A converters of identical characteristics as in the case of conventional devices.

Claims

1. A D/A conversion circuit comprising a polarity reversal means for reversing the polarities of

data in a series of input digital data group with every other data block and for supplying these data to a D/A converter, sample-hold means for holding two conversion output levels corresponding to adjacent input digital data blocks of said D/A converter, and a subtraction means for obtaining a level difference between said two conversion output levels.

2. A D/A conversion circuit comprising a positive and negative data creation means for obtaining reversed data obtained by reversing the polarities of data in a series of input digital data group and for alternately supplying the data in said input digital data group and the reversed data corresponding to these digital data, sample-hold means for holding two conversion output levels corresponding to adjacent input digital data blocks in said D/A converter, and a subtraction means for obtaining a level difference between the two conversion output levels.

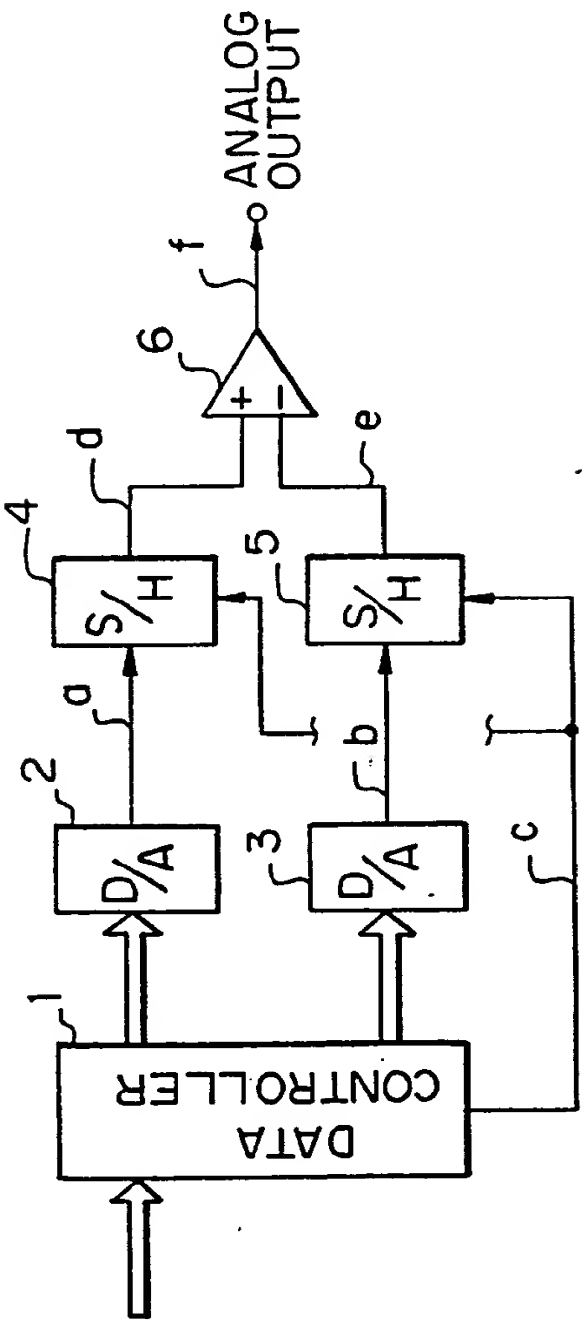


Fig. 1

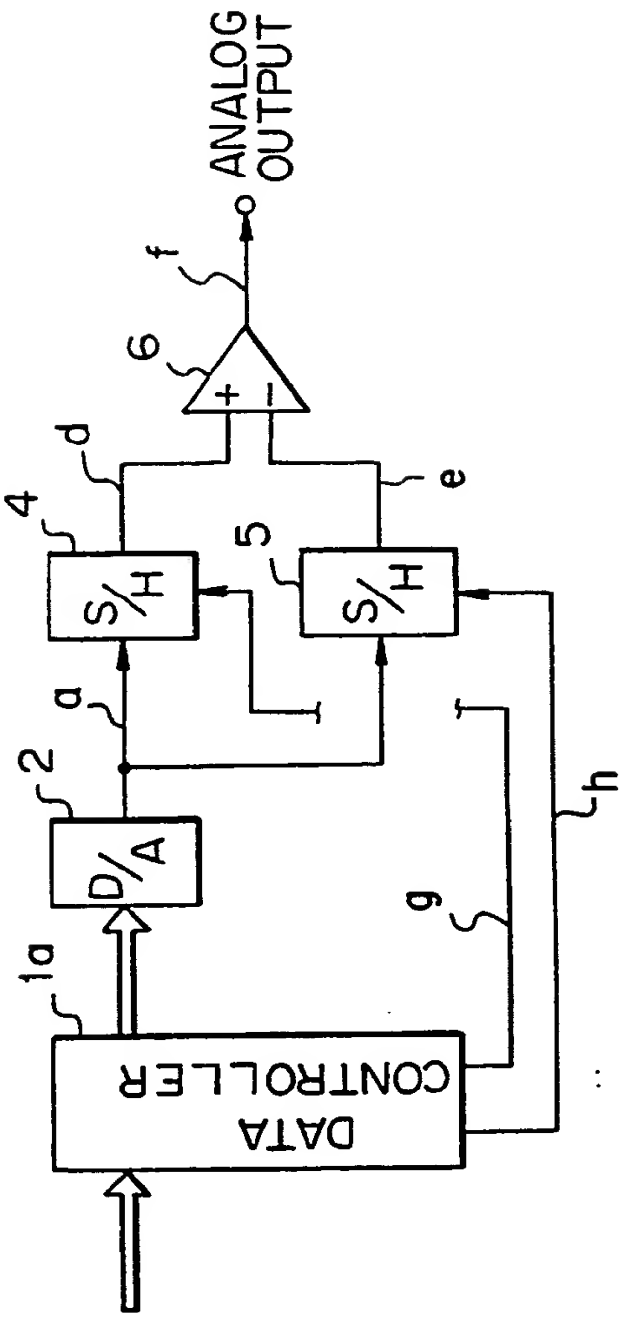


Fig. 3

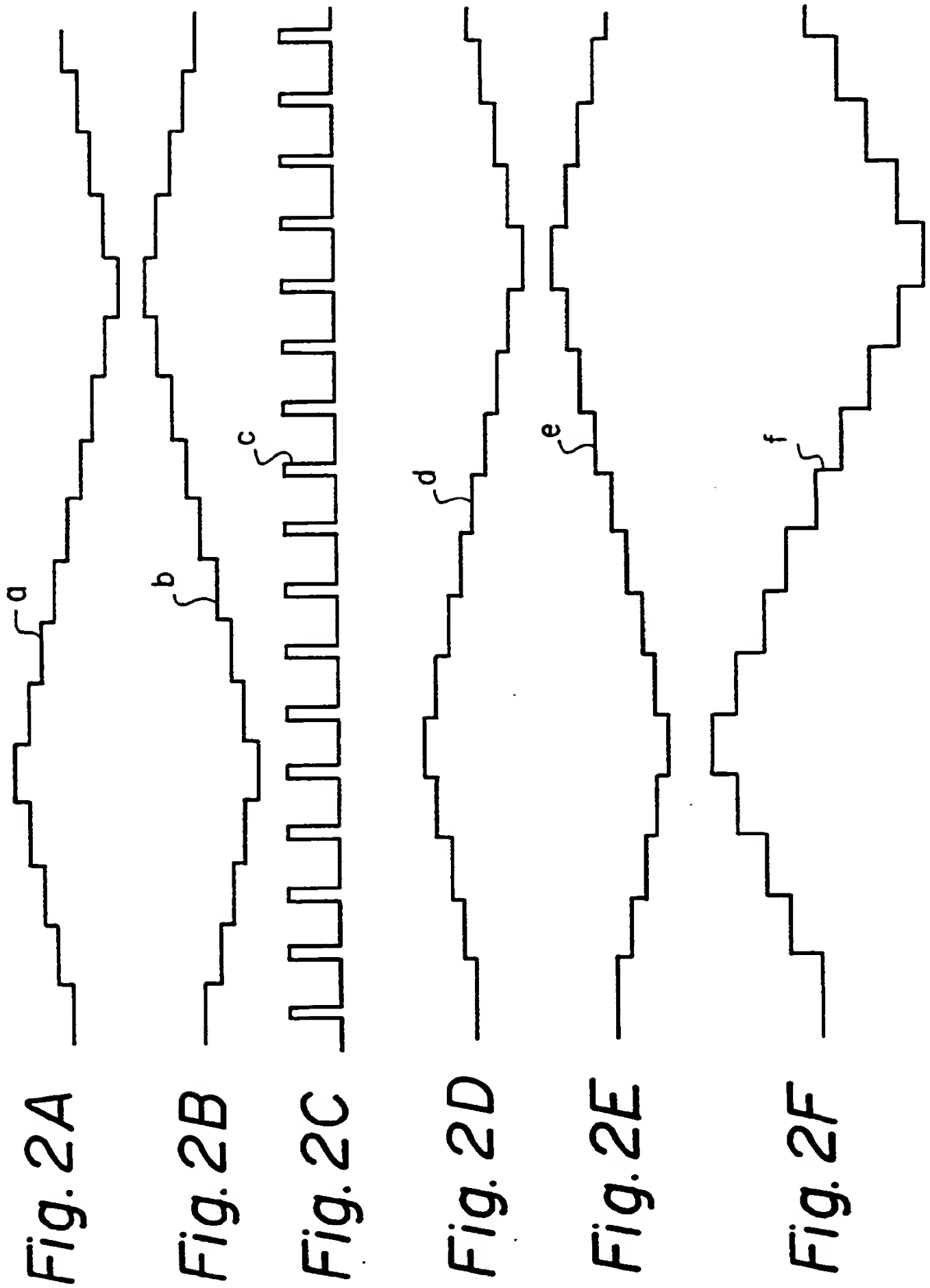


Fig. 2A

Fig. 2B

Fig. 2C

Fig. 2D

Fig. 2E

Fig. 2F

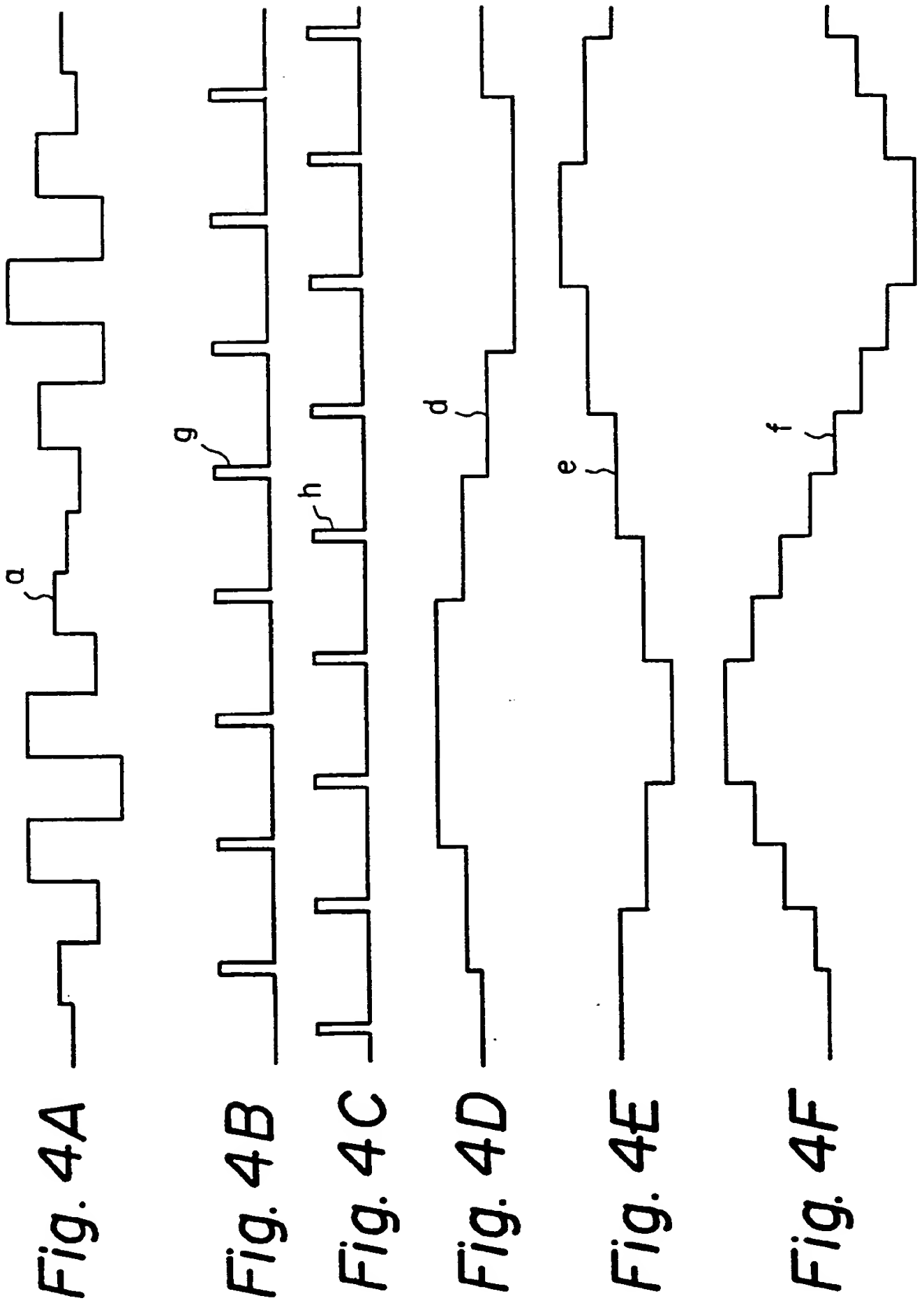


Fig. 4A

Fig. 4B

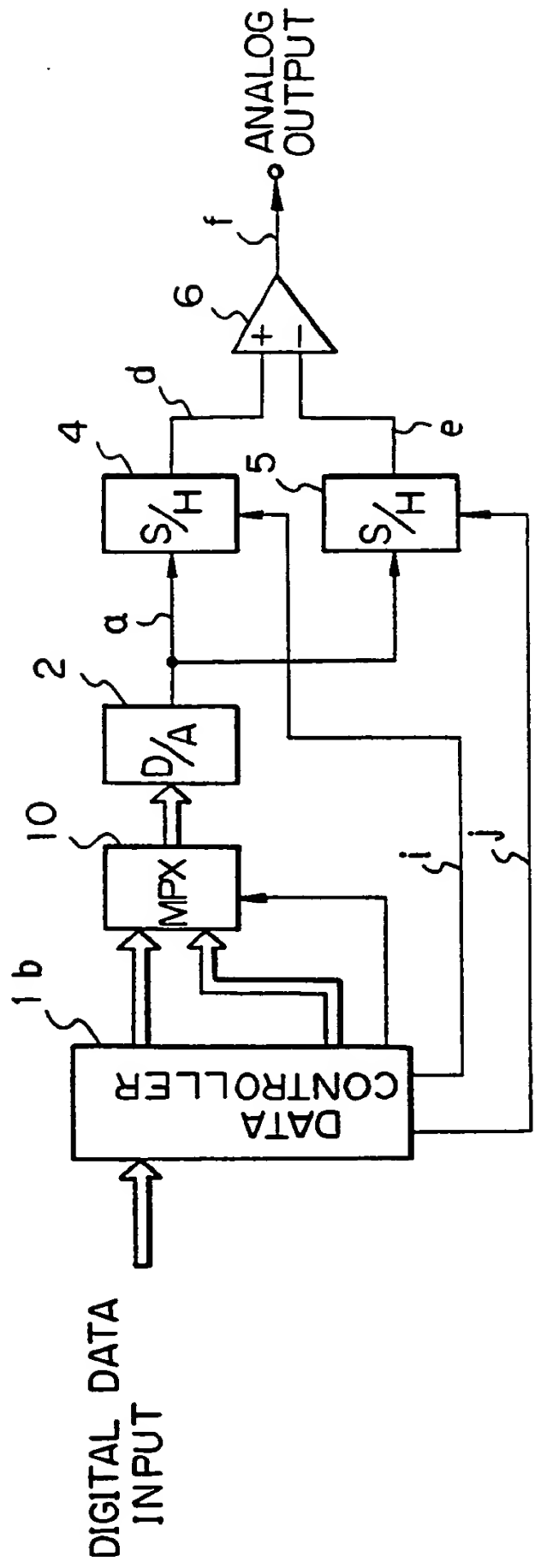
Fig. 4C

Fig. 4D

Fig. 4E

Fig. 4F

Fig. 5



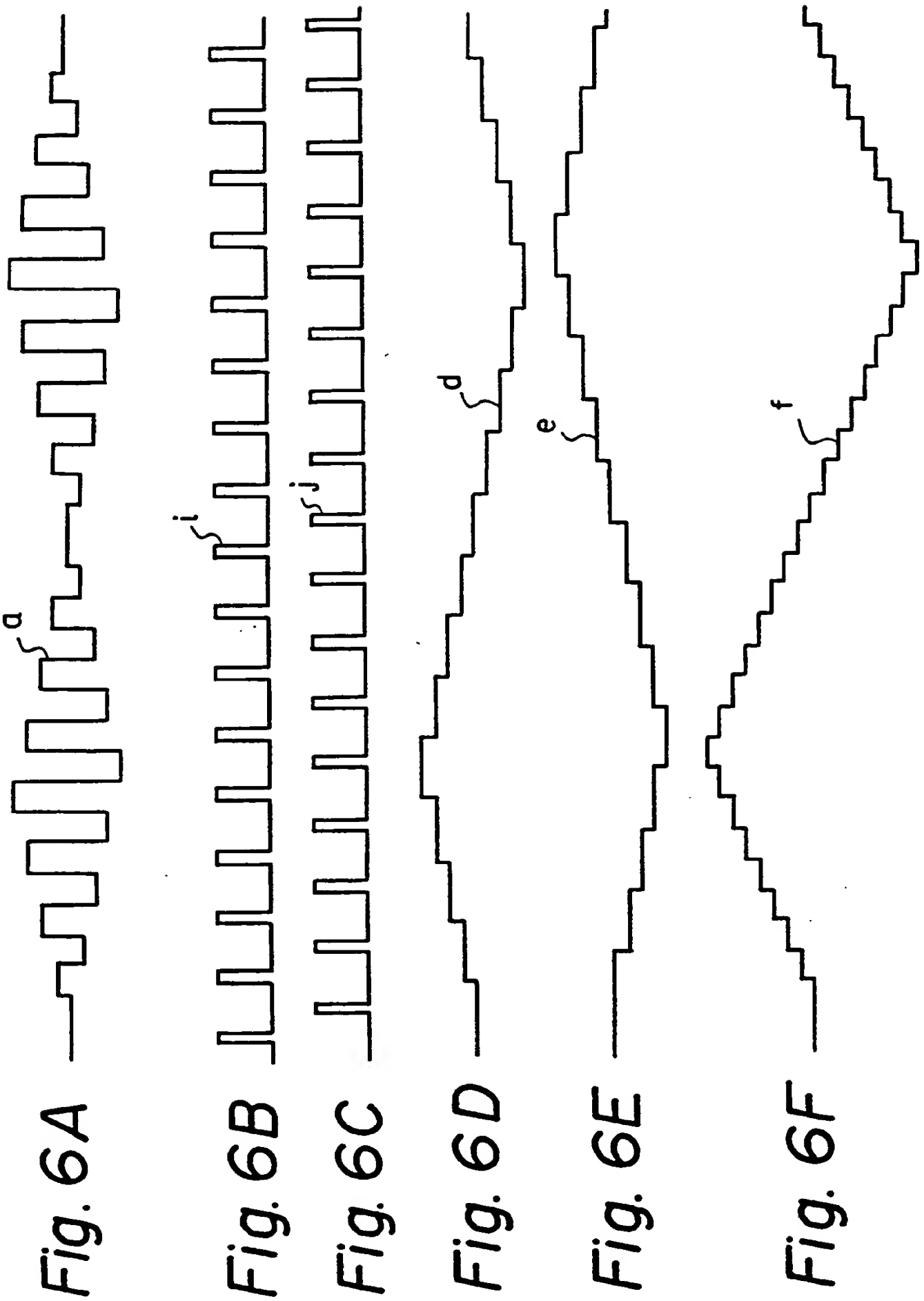


Fig. 6A

Fig. 6B

Fig. 6C

Fig. 6D

Fig. 6E

Fig. 6F

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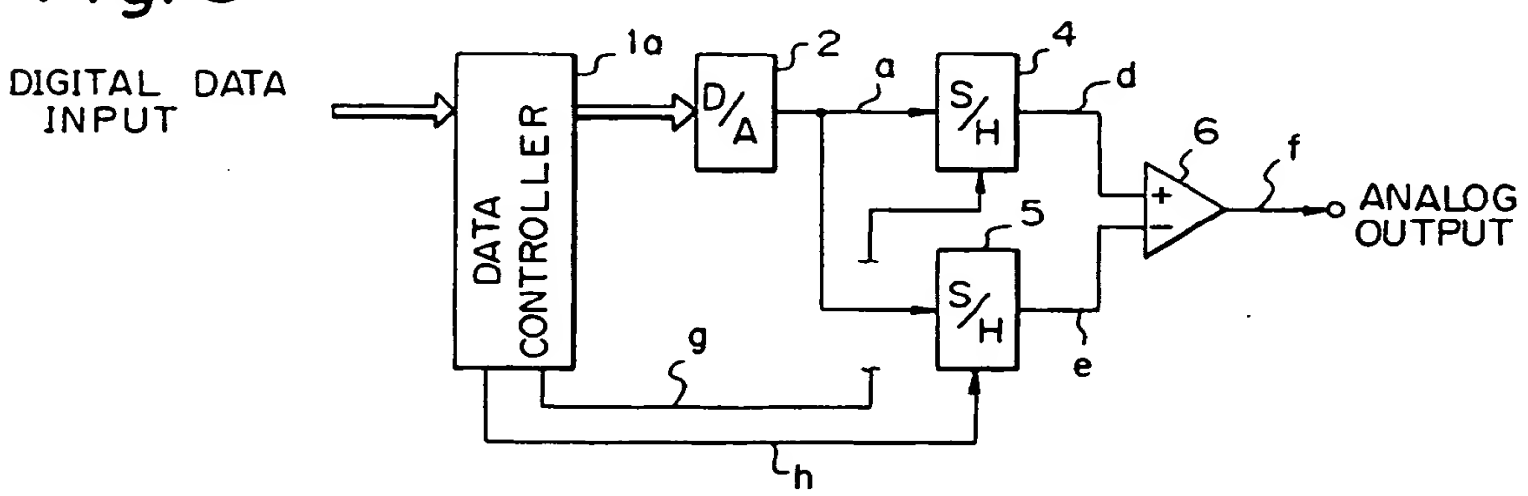

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EUROPEAN SEARCH REPORT

Application Number

EP 89 31 2356

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.5)
A	EP-A-0 170 224 (NEC) * page 11, line 24 - page 20, line 14; figure 2 *	1	H03M1/66
A	US-A-4 815 131 (OKAMOTO) * column 1, line 23 - column 1, line 56; figure 7 *	1	
A	PATENT ABSTRACTS OF JAPAN vol. 9, no. 288 (E-358)(2011) 15 November 1985 & JP-A-60 130 219 (PIONEER) 11 July 1985 * abstract *	1	

TECHNICAL FIELDS SEARCHED (Int. Cl.5)

H03M
G11B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	27 OCTOBER 1992	GUIVOL Y.

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